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Sir:
Masakatsu Saka residing at 3-3-5 Owa, Suwa City , Nagano-ken 392-8502, Japan declares:

(1) that he knows well both the Japanese and English languages;

(2) that he translated the Japanese document entitled "SOLID-STATE IMAGING DEVICE" from Japanese to English;

(3) that the attached English translation is a true and correct translation of the above-identified Japanese document to the best of his knowledge and belief; and

(4) that all statements made of his own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

Dated: July 11, 2005

[Document] Specification

[Title of the Invention] SOLID-STATE IMAGING DEVICE

[Claims]

[Claim 1]

A solid-state imaging device, comprising:

a pixel array having a plurality of pixels arranged in a matrix; and

a control unit that controls the pixel array, wherein:

the pixels each including:

a photo diode unit that generates carriers depending on intensity of incident light;

an accumulation part in which the generated carriers are accumulated;

an insulated-gate output transistor unit that outputs a signal according to threshold voltage that changes depending on the number of the carriers accumulated in the accumulation part; and

an insulated-gate clear transistor unit that discharges the carriers accumulated in the accumulation part, one of semiconductor regions that form the photo diode unit and the accumulation part functioning as a source region of the clear transistor unit;

the control unit applies predetermined voltage to a gate electrode of the clear transistor unit in an accumulation period when the generated carriers are accumulated in the accumulation part, the predetermined voltage being different from voltage applied to the gate electrode of the clear

transistor unit in a discharging period when the carries accumulated in the accumulation part are discharged; and

the clear transistor unit, if the generated carriers spill from the source region of the clear transistor unit in the accumulation period, discharges the spilled carriers through the clear transistor unit in order to prevent the spilled carriers from entering the accumulation part of adjacent pixels.

[Claim 2]

The solid-state imaging device according to Claim 1, wherein:

the clear transistor unit includes a substrate region that is formed below the gate electrode of the clear transistor unit; and

the substrate region includes:

an upper region that is formed in the vicinity of the gate electrode of the clear transistor unit and that has a relatively low impurity concentration; and

a lower region that is formed below the upper region and that has a relatively high impurity concentration.

[Claim 3]

The solid-state imaging device according to Claim 1, wherein:

the pixels each further includes:

a pixel-forming region of a second conductivity type that is formed on a semiconductor substrate of a first conductivity type and where one of the pixels is formed;

a buried region of the first conductivity type that is formed inside

the pixel-forming region and that includes a first partial buried region formed at a relatively deep position and having a relatively low impurity concentration and a second partial buried region formed at a relatively shallow position and having a relatively high impurity concentration, a junction region between the first partial buried region and the pixel-forming region forming the photo diode unit, the second partial buried region forming the accumulation part; and

a discharging region of the first conductivity type that is formed in the pixel-forming region and into which carriers discharged from the accumulation part flow;

the output transistor unit includes a gate electrode that is formed over the pixel-forming region above the accumulation part with an insulating film therebetween; and

the clear transistor unit includes a gate electrode that is formed over the pixel-forming region between the buried region and the discharging region with an insulating film therebetween.

[Claim 4]

The solid-state imaging device according to Claim 3, wherein:

the first gate electrode has a substantially annular shape; and

the output transistor unit includes a source region that is formed inside the first gate electrode and a drain region that is formed outside the first gate electrode.

[Claim 5]

The solid-state imaging device according to Claim 3, wherein:

the first conductivity type is a p-type;

the second conductivity type is an n-type; and

the carriers are holes.

[Detailed Description]

[0001]

[Field of the Invention]

The present invention relates to a solid-state imaging device of a threshold voltage modulation system.

[0002]

[Related Art]

In recent years, mobile electronic equipment such as cellular phones and digital cameras are equipped with a small solid-state imaging device. As such a solid-state imaging device, a MOS solid-state imaging device of a threshold voltage modulation system has been developed.

[0003]

The MOS solid-state imaging device of a threshold voltage modulation system includes a plurality of pixels arranged in a matrix. Each of the pixels includes a single of photo diode and a single of transistor. An accumulation part referred to as a hole pocket, where holes tend to be collected, is formed below a gate electrode of the transistor. The photo diode generates holes depending on the intensity of incident light. The generated holes are accumulated in the accumulation part. The threshold voltage of the transistor changes depending on the number of holes accumulated in the accumulation part. Then, pixel data depending on the intensity of incident light is obtained by reading out the source voltage that changes in response to the change of the threshold voltage. Using a

plurality of pixel data corresponding to the plurality of pixels allows one image data to be produced.

[0004]

Details about the MOS solid-state imaging device of a threshold voltage modulation system are disclosed in, for example, Patent Document 1 below, for example.

[0005]

[Patent Document 1]

Japanese Unexamined Patent Application Publication No. 11-195778

[0006]

[Problem to Be Solved]

Meanwhile, in a MOS solid-state imaging device of a threshold voltage modulation system, holes already existing in an accumulation part are discharged (cleared) before an image is picked up, in other words, holes are accumulated in an accumulation part. Holes in an accumulation part were conventionally discharged toward the depth direction of a substrate by applying relatively high voltage to a gate electrode of a transistor.

[0007]

In the conventional method, however, there has been a problem where discharging holes in the accumulation part is relatively difficult.

[0008]

In view of the above problem of the conventional art, this invention

is intended to provide a technique where carriers in an accumulation part can be easily discharged.

[0009]

[Means to Solve the Problem and Operation]

In order to solve at least a part of the above-described problem, a device of the present invention is a solid-state imaging device that includes a pixel array having a plurality of pixels arranged in a matrix, and a control unit that controls the pixel array. The pixels each includes a photo diode unit that generates carriers depending on the intensity of incident light, an accumulation part in which the generated carriers are accumulated, and an insulated-gate output transistor unit that outputs a signal according to threshold voltage that changes depending on the number of the carriers accumulated in the accumulation part. The pixels each also includes an insulated-gate clear transistor unit that discharges the carriers accumulated in the accumulation part, one of semiconductor regions that form the photo diode unit and the accumulation part functioning as a source region of the clear transistor unit. The control unit applies predetermined voltage to a gate electrode of the clear transistor unit in an accumulation period when the generated carriers are accumulated in the accumulation part. Here, the predetermined voltage is different from voltage applied to the gate electrode of the clear transistor unit in a discharging period when carries accumulated in the accumulation part are discharged. In the accumulation period, if the generated carriers spill from the source region of

the clear transistor unit, the clear transistor unit discharges the spilled carriers through the clear transistor unit in order to prevent the spilled carriers from entering the accumulation part of adjacent pixels.

[0010]

In this device, each of the pixels has the clear transistor unit, so that carriers in the accumulation part can be easily discharged through the clear transistor unit in the discharging period.

[0011]

Furthermore, in this device, excess carriers spilled from the source region can be discharged through the clear transistor unit in the accumulation period such that the deterioration of image quality can be avoided.

[0012]

In the device, the clear transistor unit may include a substrate region that is formed below the gate electrode of the clear transistor unit. The substrate region may include an upper region that is formed in the vicinity of the gate electrode of the clear transistor unit and that has a relatively low impurity concentration, and a lower region that is formed below the upper region and that has a relatively high impurity concentration.

[0013]

This enables the threshold voltage of the clear transistor unit to be set relatively low. As a result, discharging of excess carriers in the accumulation period can be realized.

[0014]

Preferably in the device, each of the pixels preferably includes a pixel-forming region of a second conductivity type that is formed on a semiconductor substrate of a first conductivity type and where one of the pixels is formed, and a buried region of the first conductivity type that is formed inside the pixel-forming region. The buried region includes a first partial buried region formed at a relatively deep position and having a relatively low impurity concentration, and a second partial buried region formed at a relatively shallow position and having a relatively high impurity concentration. A junction region between the first partial buried region and the pixel-forming region forms the photo diode unit. The second partial buried region forms the accumulation part. Each of the pixels also includes a discharging region of the first conductivity type that is formed in the pixel-forming region and into which carriers discharged from the accumulation part flow. The output transistor unit includes a gate electrode that is formed over the pixel-forming region above the accumulation part with an insulating film therebetween. The clear transistor unit includes a gate electrode that is formed over the pixel-forming region between the buried region and the discharging region with an insulating film therebetween.

[0015]

This can make the structure of the pixels relatively simple. Specifically, the buried region functions as the accumulation part as well as one of semiconductor regions of the photo diode unit. In addition, the

buried region also functions as the source region of the clear transistor unit.

[0016]

Preferably in the device, the first gate electrode has a substantially annular shape. The output transistor unit includes a source region that is formed inside the first gate electrode and a drain region that is formed outside the first gate electrode.

[0017]

This can further simplify the structure of the pixels.

[0018]

In the device, the first conductivity type may be a p-type, and the second conductivity type may be an n-type. The carriers may be holes.

[0019]

This enables each of the pixels to accumulate holes generated in the photo diode unit in the accumulation part.

[0020]

[Description of Embodiments]

Next, embodiments of the present invention will be described based on examples in the following order.

A. Comparative example:

A-1. Structure of solid-state imaging device of comparative example:

A-2. Operation of solid-state imaging device of comparative example:

A-3. Problems of comparative example:

B. Example:

B-1. First example:

B-2. Second example:

[0021]

A. Comparative example:

In order to explain a solid-state imaging device of examples, a solid-state imaging device of a comparative example will be described first.

[0022]

A-1. Structure of solid-state imaging device of comparative example:

Fig. 1 is an explanatory diagram showing the whole structure of a solid-state imaging device as the comparative example. A solid-state imaging device 100 includes a pixel array 110 having a plurality of pixels 112 that are arranged in a matrix, a timing-control circuit 120, a row-control circuit 130, a column-control circuit 140, and an output circuit 150.

[0023]

The timing-control circuit 120 provides a timing signal becoming the standard of operation to the row-control circuit 130 and the column-control circuit 140. The row-control circuit 130 can select a single row among a plurality of rows in response to the given timing signal. Meanwhile, the column-control circuit 140 can select a single column among a plurality of columns in response to the given timing signal. This enables any one of pixels to be selected among the plurality of pixels arranged in a matrix, and thereby a signal can be read out from the selected pixel.

[0024]

Fig. 2 is an explanatory diagram showing the internal structures of the pixel array 110, the row-control circuit 130, and the column-control circuit 140, of Fig. 1. Fig. 2, however, is represented with focus on only one of the pixels 112.

[0025]

As shown in the diagram, each of the pixels 112 includes a photo diode PD, an output transistor PTr, and a clear transistor CTr. Furthermore, a hole pocket HP where holes tend to be collected is formed below a gate electrode of the output transistor PTr.

[0026]

A drain region of the output transistor PTr is electrically coupled to a cathode of the photo diode PD and a substrate region of the clear transistor CTr (namely, a semiconductor region below a gate electrode of the clear transistor). Meanwhile, a source region of the clear transistor CTr is electrically coupled to an anode of the photo diode PD and a substrate region of the output transistor PTr that includes the hole pocket HP (namely, a semiconductor region below a gate electrode of the output transistor).

[0027]

The gate electrode, the drain region, and a source region of the output transistor PTr will be also referred to as "output gate", "output drain", and "output source" hereinafter, respectively. In addition, the gate electrode, a drain region, and the source region of the clear transistor CTr will be also referred to as "clear gate", "clear drain", and "clear source" hereinafter, respectively.

[0028]

The photo diode PD generates pairs of electrons and holes by photoelectrically converting incident light. The number of generated pairs of electrons and holes becomes larger as the intensity of incident light becomes stronger. In the hole pocket HP holes generated in the photo diode PD are accumulated. The threshold voltage of the output transistor PTr changes depending on the number of holes accumulated in the hole pocket HP. As a result, the output transistor PTr can output source voltage depending on the intensity of incident light. Then, the clear transistor CTr discharges holes accumulated in the hole pocket HP. More details about the operation of the pixels will be described later.

[0029]

The row-control circuit 130 includes an output-gate-control unit 132 for applying voltage to the gate electrode of the output transistor PTr, and an output-drain-control unit 134 for applying voltage to the drain region of the output transistor PTr. Furthermore, the row-control circuit 130 includes a clear-gate-control unit 136 for applying voltage to the gate electrode of the clear transistor CTr, and a clear-drain-control unit 138 for applying voltage to the drain region of the clear transistor CTr. In the comparative example, however, the drain voltage of the output transistor PTr is maintained at about 3.3V, while the drain voltage of the clear transistor CTr is maintained at ground potential (about 0V). The row-control circuit 130 therefore changes only the gate voltage of the output transistor PTr and the gate voltage of the clear transistor CTr in practice.

[0030]

The column-control circuit 140 includes a line memory 142 for an accumulation signal, a line memory 144 for an offset signal, and a horizontal shift register 146. The column-control circuit 140, at the time of a reading-out state, reads out signal voltage that is obtained reflecting the number of accumulated holes. The output circuit 150 amplifies the signal voltage applied from the column-control circuit 140 so as to output it as pixel data.

[0031]

Specifically, the column-control circuit 140 reads out two kinds of signal voltages from each of the pixels so as to provide them to the output circuit 150. One of the signal voltages is voltage depending on the intensity of incident light. The other of the signal voltages is voltage depending on the number of holes that remain in the hole pocket after holes accumulated therein were cleared. In the present specification, this voltage, which includes a noise component, is referred to as offset voltage. Then, the output circuit 150 amplifies the difference between these two kinds of signal voltages so as to output it as pixel data.

[0032]

As is apparent from the above explanation, the circuits 120, 130, and 140 of the comparative example correspond to the control unit of the present invention.

[0033]

Fig. 3 is an explanatory diagram graphically showing the layout of

one of the pixels 112. Fig. 4 is an explanatory diagram graphically showing a sectional view of one of the pixels 112. Here, Fig. 4 shows a sectional view along the A-A' line of Fig. 3.

[0034]

The pixels 112 are formed on a semiconductor substrate 200 of a p-type (Fig. 4). An n-region 210 composed of n-type semiconductor is formed on the substrate 200, and a first p-region 220 composed of p-type semiconductor is buried inside the n-region 210. Namely, the first p-region 220 is a floating region, which does not have an electrical contact point directly coupled to the outside. The first p-region 220 includes a first partial p-region 221a that is formed at a relatively deep position and that has a relatively low impurity concentration, and a second partial p-region 222b that is formed at a relatively shallow position and that has a relatively high impurity concentration. In addition, a second p-region 230 is formed in an end of the n-region 210.

[0035]

A junction part between the n-region 210 and the first p-region 220 forms the photo diode PD.

[0036]

The output transistor PTr (Fig. 4) is a depletion type n-channel MOS transistor. The output transistor PTr is formed on a semiconductor substrate whose surface has the n-region 210 provided thereon. In order to suppress the generation of holes causing noise by filling the trap level existing in the surface of the semiconductor substrate with electrons, an

n-region is formed on the surface of the semiconductor substrate. A substantially annular output gate 270P is formed over the n-region 210 with a substantially annular gate oxide film 260P therebetween. The inside of the substantially annular output gate 270P functions as the source region of the output transistor PTr, while the outside thereof functions as the drain region of the output transistor PTr. Meanwhile, the first p-region 220 formed below the output gate 270P is an electrically floating region surrounded by the n-region, and functions as a region (a substrate region) that applies substrate potential to the output transistor PTr. In Figs. 3 and 4, a source contact region 210s and a drain contact region 210d are shown. These regions are coupled to a metal wiring and have relatively high impurity concentrations. Although Figs. 3 and 4 show the case where the drain contact region 210d is formed in one of the pixels 112, it is formed for the plurality of pixels 112 in common practically.

[0037]

The hole pocket HP is formed of the second partial p-region (p+ region) 222b whose impurity concentration is relatively high. The hole pocket HP has a substantially annular shape and is formed below the substantially annular output gate 270P.

[0038]

Here, in Fig. 4, the hole pocket HP is represented at a position relatively deep from the surface of the substrate 200 for convenience. Practically, it is formed at a position relatively shallow from the surface of the substrate 200. In addition, although the hole pocket HP is represented

so that it has relatively large thickness in the diagram, it practically has relatively small thickness.

[0039]

The clear transistor CTr (Fig. 4) is an enhancement type p-channel MOS transistor. A clear gate 270C is formed over the n-region 210 with a gate oxide film 260C therebetween. The first p-region 220, which includes the hole pocket HP, functions as the source region of the clear transistor CTr. The second p-region 230, which faces the first p-region 220 with the clear gate 270C therebetween, functions as the drain region of the clear transistor CTr. Meanwhile, the n-region 210 formed below the clear gate 270C functions as the substrate region of the clear transistor CTr. In Figs. 3 and 4, a drain contact region 230d that is coupled to a metal wiring and whose impurity concentration is relatively high, is shown.

[0040]

The voltage of the substrate 200 is maintained at ground potential (about 0V). Meanwhile, the drain voltage of the output transistor PTr is maintained at about 3.3V as previously described. In the comparative example, therefore, the n-region 210 functions as a pixel-isolating region that suppresses electrical interference between pixels adjacent to each other.

[0041]

The first p-region 220 functions as the hole pocket HP as well as the anode of the photo diode PD as previously described. In addition, the first p-region 220 functions as the source region of the clear transistor CTr as

well as the substrate region of the output transistor PTr. Such a structure enables the structure of the pixel to be simplified. The pixels 112 may be formed by doping impurity ions into a semiconductor substrate, or may be formed by epitaxial growth.

[0042]

As is apparent from the above explanation, the n-region 210, the first p-region 220, and the second p-region 230 of the comparative example correspond to the pixel-forming region, the buried region, and the discharging region of the present invention, respectively.

[0043]

A-2. Operation of solid-state imaging device of comparative example:

Fig. 5 is an explanatory diagram showing the operational sequence of the pixels 112. As shown in the diagram, one time of the operational sequence is completed through a first clear period T1, an accumulation period T2, a reading-out period T3 for an accumulation signal, a second clear period T4, and a reading-out period T5 for an offset signal. The two clear periods T1 and T4 are periods for discharging holes from the hole pocket HP. The accumulation period T2 is a period for accumulating holes in the hole pocket HP. The two reading-out periods T3 and T5 are periods for reading out a signal depending on the number of holes existing in the hole pocket HP.

[0044]

In the comparative example, drain voltage PVd of the output transistor PTr is consistently maintained at about 3.3V, while drain voltage

CVd of the clear transistor CTr is consistently maintained at about 0V as previously described. The way of controlling the transistors PTr and CTr during the clear period T1 is the same as that during the clear period T4, and the way of controlling the transistors PTr and CTr during the reading-out period T3 is the same as that during the reading-out period T5.

[0045]

A-2-1. Clear period:

Fig. 6 is an explanatory diagram showing the internal state of one of the pixels 112 during the first clear period T1. In the first clear period T1, gate voltage PVg of the output transistor PTr is set to be about 0V, while source voltage PVs to be about 3.3V as shown in Fig. 5. At this time, the output transistor PTr is set to be in an "off" state. Meanwhile, gate voltage CVg of the clear transistor CTr is set to be about 0V. At this time, the clear transistor CTr is set to be in an "on" state. This is because the substrate voltage of the clear transistor CTr (namely, the voltage of the n-region 210 below the clear gate 270C) is almost equal to the drain voltage PVd (about 3.3V) of the output transistor PTr.

[0046]

In the clear period T1, a channel region 210c is formed below the clear gate 270C. Holes existing in the hole pocket HP therefore pass through the first p-region 220, the channel region 210c, and the second p-region 230 so as to be discharged from the drain contact region 230d.

[0047]

The operation during the fourth clear period T4 (Fig. 5) is the same

as that during the first clear period T1. The first clear period T1, however, is set in order to discharge holes that may slightly remain in the hole pocket HP preceding the accumulation period T2, while the second clear period T4 is set in order to discharge holes that are accumulated in the hole pocket HP during the accumulation period T2.

[0048]

A-2-2. Accumulation period:

Fig. 7 is an explanatory diagram showing the internal state of one of the pixels 112 during the accumulation period T2. In the accumulation period T2, the gate voltage PVg of the output transistor PTr is changed as shown in Fig. 5. Specifically, the gate voltage PVg is set to be about 3.3V. At this time, the output transistor PTr is set to be in an "on" state. In addition, the gate voltage CVg of the clear transistor CTr is also changed. Specifically, the gate voltage CVg is set to be about 3.3V. At this time, the clear transistor CTr is set to be in an "off" state.

[0049]

If the output transistor PTr is set to be in an "on" state as described above, an electronic layer can be induced in the interface of the gate insulating film. As a result, the generation of dark currents attributed to interface defects can be suppressed.

[0050]

In the accumulation period T2, a depletion region (for example, a region sandwiched between two dashed lines of Fig. 7) is formed in the vicinity of the junction interface between the n-region 210 and the p-region

220 that form the photo diode PD. When light enters the photo diode PD, pairs of electrons and holes are generated by photoelectrical conversion. Electrons pass through the n-region 210 so as to be discharged from the drain contact region 210d. Meanwhile, holes are collected in the hole pocket HP in the p-region 220 so as to be accumulated. This is because the hole pocket HP has a relatively high impurity concentration such that it has relatively low potential against holes.

[0051]

A-2-3. Reading-out period:

Fig. 8 is an explanatory diagram showing the internal state of one of the pixels 112 during the reading-out period T3 for an accumulation signal. In the reading-out period T3 for an accumulation signal, the gate voltage PVg of the output transistor PTr is changed as shown in Fig. 5. Specifically, the gate voltage PVg is set to be about 2V, which is lower than the drain voltage PVd (about 3.3V). In addition, the output transistor PTr operates as a source follower in the reading-out period T3 for an accumulation signal. Then, accumulation voltage (an accumulation signal) depending on the number of holes accumulated in the hole pocket HP is read out from the source region of the output transistor PTr.

[0052]

In the reading-out period T3 for an accumulation signal, holes are maintained at a state of being accumulated in the hole pocket HP. The source voltage PVs of the output transistor PTr is represented by a formula "PVs = PVg - Vth", where Vth is the threshold voltage of the output

transistor PTr. The threshold voltage Vth changes depending on the number of holes accumulated in the hole pocket HP. Specifically, the larger the number of accumulated holes is, the lower the threshold voltage Vth becomes. Meanwhile, the lower the threshold voltage Vth is, the higher the source voltage PVs becomes. Namely, the larger the number of holes accumulated in the hole pocket HP is, in other words, the higher the intensity of light entering the photo diode PD is, the higher the source voltage PVs becomes.

[0053]

The operation during the reading-out period T5 for an offset signal (Fig. 5) is the same as that during the reading-out period T3 for an accumulation signal. In the reading-out period T5 for an offset signal, however, offset voltage (an offset signal) of a state where holes scarcely exist in the hole pocket HP is output from the source region of the output transistor PTr. The output circuit 150 (Fig. 1) amplifies difference between read-out two signals (namely, an accumulation signal and an offset signal) so as to output pixel data from which a noise component is removed.

[0054]

Here, although the second clear period T4 and the reading-out period T5 for an offset signal are included in one time of the operational sequence in the comparative example as shown in Fig. 5, these two periods T4 and T5 may be omitted. In this case, the output circuit 150 (Fig. 1) may obtain pixel data from difference between a read-out accumulation signal and a predetermined offset signal that is previously prepared. Otherwise,

the output circuit 150 may obtain pixel data from only a read-out accumulation signal.

[0055]

As described above, the solid-state imaging device 100 of the comparative example includes the pixel array 110 having the plurality of pixels 112 arranged in a matrix. In addition, each of the pixels includes the photo diode PD for generating holes according to the intensity of incident light, and the hole pocket HP for accumulating the generated holes. Each of the pixels also includes the output transistor PTr for outputting a signal according to the threshold voltage that changes depending on the number of holes accumulated in the hole pocket, and the clear transistor CTr for discharging holes accumulated in the hole pocket. Thus, in the solid-state imaging device 100 of the comparative example, each of the pixels 112 has the clear transistor CTr such that holes in the hole pocket can be easily discharged through its channel region 210c.

[0056]

Each of the pixels heretofore does not have the clear transistor as previously described. For this reason, holes were discharged toward the depth direction of the substrate 200 by applying relatively high voltage (for example, from about 5V to about 7V) to the gate electrode of the output transistor PTr. Namely, the row-control circuit 130 (Fig. 1) was required to generate relatively high voltage.

[0057]

On the other hand, in the comparative example, holes can be

discharged through the channel region 210c formed in the vicinity of the surface of the substrate 200 by only controlling the clear transistor with relatively low voltage, since each of the pixels includes the clear transistor CTr. Holes in the hole pocket HP therefore can be easily discharged.

[0058]

A-3. Problems in comparative example

Meanwhile, in the comparative example, if light with strong intensity enters a part of the pixels of the pixel array in the accumulation period T2 (Fig. 5), a phenomenon where the distribution of entering light on the pixel array mismatches the distribution of the pixel data output from the pixel array, may be caused.

[0059]

Fig. 9 is an explanatory diagram showing the internal state of one of the pixels 112 at the time of receiving light with strong intensity during the accumulation period T2. Fig. 9 (A) shows a sectional view along the B-B' line of Fig. 3. In Fig. 9 (A), however, one of the pixels 112 where light enters (pixels of interest), and adjacent pixels 112' that are arranged in the same row as that of the pixels of interest, are shown. Fig. 9 (B) shows the potential distribution along the C line of Fig. 9 (A). The curved line of Fig. 9 (B), however, shows the potential distribution at a state where holes are not accumulated. As is apparent from the curved line, the potential of the first p-region 220 is lower than that of the n-region 210 surrounding it. In addition, inside the first p-region 220, the potential of the second partial p-region (p+ region) 222b, which forms the hole pocket HP, is lower than

that of the first partial p-region 221a.

[0060]

When light enters the pixels 112 of interest, the photo diode PD generates holes. The generated holes are accumulated in the hole pocket HP. However, if the intensity of light entering the pixels 112 of interest is relatively strong, holes spill from the hole pocket HP so as to be placed in the first p-region 220, which includes the hole pocket HP. Moreover, if the intensity of light entering the pixels 112 of interest is further stronger, namely, if the number of generated holes exceeds the capacity of the first p-region 220, the excess holes spill from the first p-region 220.

[0061]

The holes spilled from the first p-region 220 enter the first p-region 220 of the adjacent pixels 112' over the barrier of the n-region 210. At this time, in the adjacent pixels 112', holes are accumulated in the hole pocket even though light does not enter them. Then, accumulation signals depending on the number of holes accumulated in the hole pocket are read out from the adjacent pixels 112'. Although Fig. 9 shows the case where excess holes enter the adjacent holes 112' that are arranged in the same row as that of the pixels 112 of interest, excess holes may also enter adjacent pixels that are arranged in rows adjacent to the pixels 112 of interest in the same manner. As a result, in a produced image, not only a region corresponding to the pixels of interest shows white, a region surrounding it also shows white such that the image quality is deteriorated. This phenomenon is referred to as "blooming".

[0062]

Examples described below employ features for avoiding the deterioration of image quality. Specifically, the generation of the blooming phenomenon is avoided by utilizing the clear transistor CTr, which is provided to each of the pixels.

[0063]

B. Examples:

Fig. 10 is an explanatory diagram showing voltages applied to four terminals of the clear transistor CTr. As previously described, the gate voltage CVg is set to be about 3.3V during the accumulation period T2 (Fig. 5) in the comparative example. The substrate voltage CVb (namely, the voltage of the n-region 210 that functions as a substrate region of the clear transistor) is set to be about 3.3V, which is almost equal to the drain voltage PVd of the output transistor. The drain voltage CVd is set to be about 0V. Meanwhile, the source voltage CVs is equal to the voltage of the first p-region 220 and depends on the number of holes generated in the photo diode PD.

[0064]

The clear transistor CTr is set to be in an "on" state when the condition "CVs > CVg + CVth" is satisfied, while being set to be an "off" state when the condition is not satisfied. Here, CVth is the threshold voltage (absolute value) of the clear transistor CTr.

[0065]

In the comparative example, the clear transistor CTr is kept at an

"off" state even when holes generated in the photo diode PD spill from the first p-region 220, in the accumulation period. On the other hand, in examples described below, the clear transistor CTr is set to be in an "on" state if generated holes spill from the first p-region 220. Namely, an adjustment is made so that the cleat transistor CTr is changed from an "off" state to an "on" state with the source voltage CVs at the time when generated holes spill from the first p-region 220. This enables the clear transistor CTr to discharge holes spilled from the first p-region 220. As a result, the generation of the blooming phenomenon can be avoided.

[0066]

B-1. First example:

In a first example, the control of the pixels is the same as that of the comparative example (Fig. 5), while only the pixel structure is different therefrom.

[0067]

Fig. 11 is an explanatory diagram showing the pixel structure of the first example and corresponds to Fig. 4. Fig. 11 is almost same as Fig. 4. In pixels 112A, however, an n-region 210A that functions as the substrate region of the clear transistor CTr is changed. Specifically, the n-region 210A formed below the clear gate 270C includes an interface region 210b having a relatively low impurity concentration in the vicinity of the interface with the gate insulating film 260C. In other words, the substrate region 210A of the clear transistor CTr includes an upper region (interface region 210b) formed in the vicinity of the clear gate 270C and having a

relatively low impurity concentration, and a lower region formed below the upper region and having a relatively high impurity concentration. In this structure, the clear transistor CTr is set to be in an "on" state with the source voltage CVs at the time when generated holes spill from the first p-region 220, since the threshold voltage CVth of the clear transistor is set to be relatively low.

[0068]

Fig. 12 is an explanatory diagram showing the internal state of one of the pixels 112A during the accumulation period T2. Figs. 12 (A) and (B) show the internal states of the pixels, at one case where the intensity of entering light is at a usual level, and at another case where it is at a high level.

[0069]

When the intensity of entering light is at a usual level (Fig. 12 (A)), holes generated in the photo diode PD are accumulated in only the hole pocket HP. At this time, the voltage of the first p-region 220, namely, the source voltage CVs of the clear transistor is, for example, from about 2V to about 3V such that the clear transistor CTr is set to be in an "off" state.

[0070]

Meanwhile, when the intensity of entering light is at a high level (Fig. 12 (B)), holes generated in the photo diode PD spill from the first p-region 220 including the hole pocket HP. At this time, the voltage of the first p-region 220, namely, the source voltage CVs of the clear transistor is, for example, about 5V such that the clear transistor CTr is set to be in an

"on" state. More specifically, when the source voltage CVs is relatively high, the channel region 210c is formed in the n-region 210 below the clear gate 270C. The excess holes spilled from the first p-region 220 pass through the channel region 210c and the second p-region 230 so as to be discharged from the drain contact region 230d. The channel region 210c is formed in the interface region 210b, which has a relatively low impurity concentration.

[0071]

As described above, the threshold voltage CVth of the clear transistor is set to be relatively low in the first example. Thus, even when the row-control circuit 130 (Fig. 1) applies predetermined voltage (in the present example, about 3.3V) to the clear gate 270C, the transition of the clear transistor CTr from an "off" state to an "on" state in accordance with the source voltage CVs is realized. Specifically, if the source voltage is relatively low (namely, generated holes do not spill from the source region 220), the clear transistor CTr is set to be in an "off" state. Meanwhile, if the source voltage is relatively high (namely, generated holes spill from the source region 220), the clear transistor CTr is set to be in an "on" state. The clear transistor CTr, therefore, can discharge excess holes through the channel region 210c if holes spill from the source region 220 of the clear transistor. As a result, spilled excess holes can be prevented from entering the hole pocket of the adjacent pixels such that the deterioration of image quality (the generation of a blooming phenomenon) can be avoided.

[0072]

Here, the predetermined voltage applied to the clear gate 270C in the accumulation period T2 (in the present example, about 3.3V) is different from the voltage applied to the clear gate 270C in the clear periods T1 and T4 (in the present example, about 0V). Namely, the gate voltage CVg is set to voltage where the channel region 210c is invariably formed during the clear periods T1 and T4, while the gate voltage CVg is set to voltage where the channel region 210c is formed depending on the state of the source region (source voltage) during the accumulation period T2.

[0073]

B-2. Second example:

In a second example, the pixel structure is the same as that of the comparative example (Fig. 4), while only the control of the pixels is different therefrom.

[0074]

Fig. 13 is an explanatory diagram showing the operational sequence of the pixels 112 in the second example and corresponds to Fig. 5. Although Fig. 13 is almost same as Fig. 5, the gate voltage CVg of the clear transistor CTr during the accumulation period T2 is changed. Specifically, the gate voltage CVg is changed to predetermined voltage Vp which is lower than about 3.3V in the comparative example (for example, about 2.5V). If the gate voltage CVg is set to the voltage Vp, which is relatively low, the clear transistor CTr is set to be in an "on" state with the source voltage CVs at the time when generated holes spill from the first p-region 220.

[0075]

Fig. 14 is an explanatory diagram showing the internal state of one of the pixels 112 during the accumulation period T2. Here, Figs. 14 (A) and (B) correspond to Figs. 12 (A) and (B), respectively. When the intensity of incident light is at a usual level (Fig. 14 (A)), as with Fig. 12 (A), the clear transistor CTr is set to be in an "off" state. Meanwhile, when the intensity of incident light is at a high level (Fig. 14 (B)), as with Fig. 12 (B), the clear transistor CTr is set to be in an "on" state. In the first example, however, the channel region 210c is formed since the impurity concentration of the interface region 210b is set to be relatively low, while in the second example, the channel region 210c is formed since the gate voltage CVg applied to the clear gate 270C is set to be relatively low.

[0076]

As described above, the gate voltage CVg of the clear transistor is set to the predetermined voltage Vp, which is relatively low, in the second example. Thus, even when the row-control circuit 130 (Fig. 1) applies predetermined voltage (in the present example, about 2.5V) to the clear gate 270C, the transition of the clear transistor CTr from an "off" state to an "on" state in accordance with the source voltage CVs is realized. Specifically, the clear transistor CTr is set to be in an "off" state when the source voltage is relatively low, while being set to be in an "on" state when it is relatively high. The clear transistor CTr, therefore, can discharge excess holes through the channel region 210c if holes spill from the source region 220 of the clear transistor. As a result, spilled excess holes can be prevented from entering the hole pocket of the adjacent pixels such that the deterioration of

image quality (the generation of a blooming phenomenon) can be avoided.

[0077]

Here, as with the first example, the predetermined voltage applied to the clear gate 270C in the accumulation period T2 (in the present example, about 2.5V) is different from the voltage applied to the clear gate 270C in the clear periods T1 and T4 (in the present example, about 0V).

[0078]

It should be understood that the present invention is not limited to the above-described examples and embodiments but applied to various kinds of modifications without departing from the scope and spirit of the present invention. For example, the following modifications are available.

[0079]

(1) Although the output transistor PTr has the substantially annular gate electrode 270P in the above-described examples, instead of this, it may have a substantially rectangular gate electrode. In the examples, however, there is an advantage that the structure of pixels can be simplified. In addition, the substantially annular gate electrode has a substantially circular outer periphery and a substantially circular inner periphery in the examples, instead of this, it may have a substantially polygonal outer periphery and a substantially polygonal inner periphery. Otherwise, it may have a substantially polygonal outer periphery and a substantially circular inner periphery. Namely, "substantially annular" has only to be a closed shape.

[0080]

(2) In the first example, the threshold voltage CVth is set to be relatively low, and thereby the switching of the clear transistor CTr between an "off" state and an "on" state in accordance with the source voltage CVs is realized in the accumulation period.

[0081]

In the second example, the gate voltage CVg is set to be relatively low, and thereby the switching of the clear transistor between an "off" state and an "on" state in accordance with the source voltage CVs is realized in the accumulation period.

[0082]

Generally, if generated carriers spill from the source region of the clear transistor unit in the accumulation period, it is sufficient that the clear transistor unit discharges the spilled carriers through the clear transistor unit in order to prevent the spilled carriers from entering the accumulation part of the adjacent pixels.

[0083]

In addition, although the threshold voltage CVth is adjusted by the impurity concentration of the interface region 210b in the first example, instead of this, it may be adjusted by the capacitance of the gate insulating film 260C.

[0084]

(3) Although holes are accumulated in the accumulation part in the examples, instead of this, electrons may be accumulated. In this case, a p-type semiconductor region and an n-type semiconductor region may be

replaced with each other.

[Brief Description of Drawings]

[Fig. 1] Fig. 1 is an explanatory diagram showing the whole structure of a solid-state imaging device as a comparative example.

[Fig. 2] Fig. 2 is an explanatory diagram showing the internal structures of the pixel array 110, the row-control circuit 130, and the-column-control circuit 140 of Fig. 1.

[Fig. 3] Fig. 3 is an explanatory diagram graphically showing the layout of one of the pixels 112.

[Fig. 4] Fig. 4 is an explanatory diagram graphically showing the sectional view of one of the pixels 112.

[Fig. 5] Fig. 5 is an explanatory diagram showing the operational sequence of the pixels 112.

[Fig. 6] Fig. 6 is an explanatory diagram showing the internal state of one of the pixels 112 during a first clear period T1.

[Fig. 7] Fig. 7 is an explanatory diagram showing the internal state of one of the pixels 112 during an accumulation period T2.

[Fig. 8] Fig. 8 is an explanatory diagram showing the internal state of one of the pixels 112 during a reading-out period T3 for an accumulation signal.

[Fig. 9] Fig. 9 is an explanatory diagram showing the internal state of one of the pixels 112 at the time of receiving light with strong intensity during the accumulation period T2.

[Fig. 10] Fig. 10 is an explanatory diagram showing voltages applied

to four terminals of the clear transistor CTr.

[Fig. 11] Fig. 11 is an explanatory diagram showing the pixel structure of the first example and corresponds to Fig. 4.

[Fig. 12] Fig. 12 is an explanatory diagram showing the internal state of one of the pixels 112A during the accumulation period T2.

[Fig. 13] Fig. 13 is an explanatory diagram showing the operational sequence of the pixels 112 in the second example and corresponds to Fig. 5.

[Fig. 14] Fig. 14 is an explanatory diagram showing the internal state of one of the pixels 112 during the accumulation period T2.

[Reference Numerals]

100 solid-state imaging device

110 pixel array

112, 112A pixels

120 timing-control circuit

130 row-control circuit

132 output-gate-control unit

134 output-drain-control unit

136 clear-gate-control unit

138 clear-drain-control unit

140 column-control circuit

142 line memory for an accumulation signal

144 line memory for an offset signal

146 horizontal shift register

150 output circuit

200 semiconductor substrate

210, 210A n-region (substrate region of clear transistor)

210b interface region

210c channel region

210d drain contact region

210s source contact region

220 first p-region (source region of clear transistor)

221a first partial p-region

222b second partial p-region

230 second p-region

230d drain contact region

260P gate insulating film

260C gate insulating film

270P output gate

270C clear gate

PTr output transistor

PVd drain voltage

PVg gate voltage

PVs source voltage

CTr clear transistor

CVd drain votage

CVg gate voltage

CVs source voltage

CVb substrate voltage

HP hole pocket

PD photo diode

[Document] Abstract

[ABSTRACT]

[Problem]

Providing a technique where carriers in an accumulation part can be easily discharged.

[Means to Solve the Problem]

A solid-state imaging device includes a pixel array having a plurality of pixels arranged in a matrix. The pixels each includes a photo diode PD that generates carriers depending on the intensity of incident light, an accumulation part HP in which the generated carriers are accumulated, an output transistor PTr that outputs a signal according to threshold voltage that changes depending on the number of the carriers accumulated in the accumulation part, and a clear transistor CTr that discharges the carriers accumulated in the accumulation part. One of semiconductor regions that form the photo diode and the accumulation part function as a source region of the clear transistor. If the generated carriers spill from the source region of the clear transistor in the accumulation period, the clear transistor discharges the spilled carriers through a channel 210c of the clear transistor in order to prevent the spilled carriers from entering the accumulation part of adjacent pixels.

[SELECTED FIGURE] Fig. 12

Translation of Drawings

FIG. 1

110 ELEMENT ARRAY, 120 TIMING-CONTROL CIRCUIT, 130 ROW-CONTROL CIRCUIT, 140 COLUMN-CONTROL CIRCUIT, 150 OUTPUT CIRCUIT

FIG. 2

132 OUTPUT-GATE-CONTROL UNIT, 134 OUTPUT-DRAIN-CONTROL UNIT, 136 CLEAR-GATE-CONTROL UNIT, 138 CLEAR-DRAIN-CONTROL UNIT, 142 LINE MEMORY FOR AN ACCUMULATION SIGNAL, 144 LINE MEMORY FOR AN OFFSET SIGNAL, 146 HORIZONTAL SHIFT REGISTER, 150 OUTPUT CIRCUIT

FIG. 5

T1: CLEAR T2: ACCUMULATION T3: READING-OUT AN ACCUMULATION SIGNAL T4: CLEAR T5: READING-OUT AN OFFSET SIGNAL

FIG. 6

CLEAR PERIOD

FIG. 7

ACCUMULATION PERIOD

FIG. 8

READING-OUT PERIOD

FIG. 9B

POTENTIAL, 220: P-REGION, 210: N-REGION

FIG. 12A

ACCUMULATION PERIOD

FIG. 12B

ACCUMULATION PERIOD

FIG. 13

T1: CLEAR T2: ACCUMULATION T3: READING-OUT AN ACCUMULATION SIGNAL T4: CLEAR T5: READING-OUT AN OFFSET SIGNAL

FIG. 14A

ACCUMULATION PERIOD

FIG. 14B

ACCUMULATION PERIOD

FIG.1

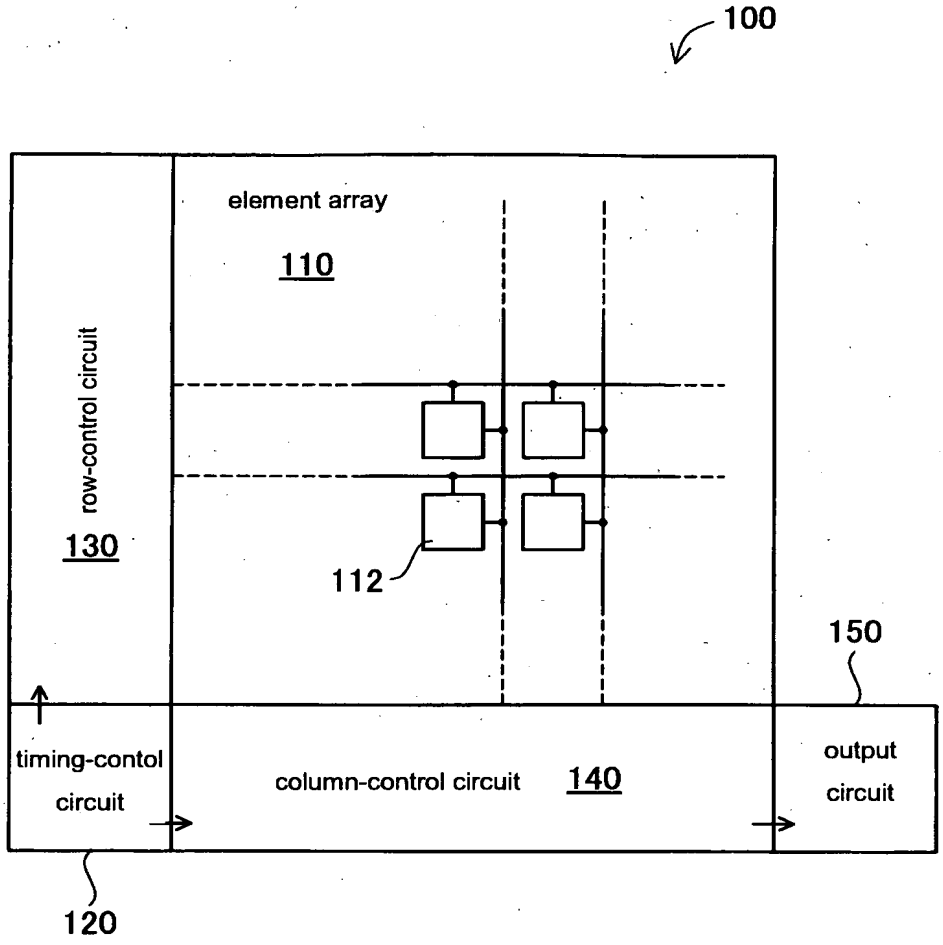

FIG.2

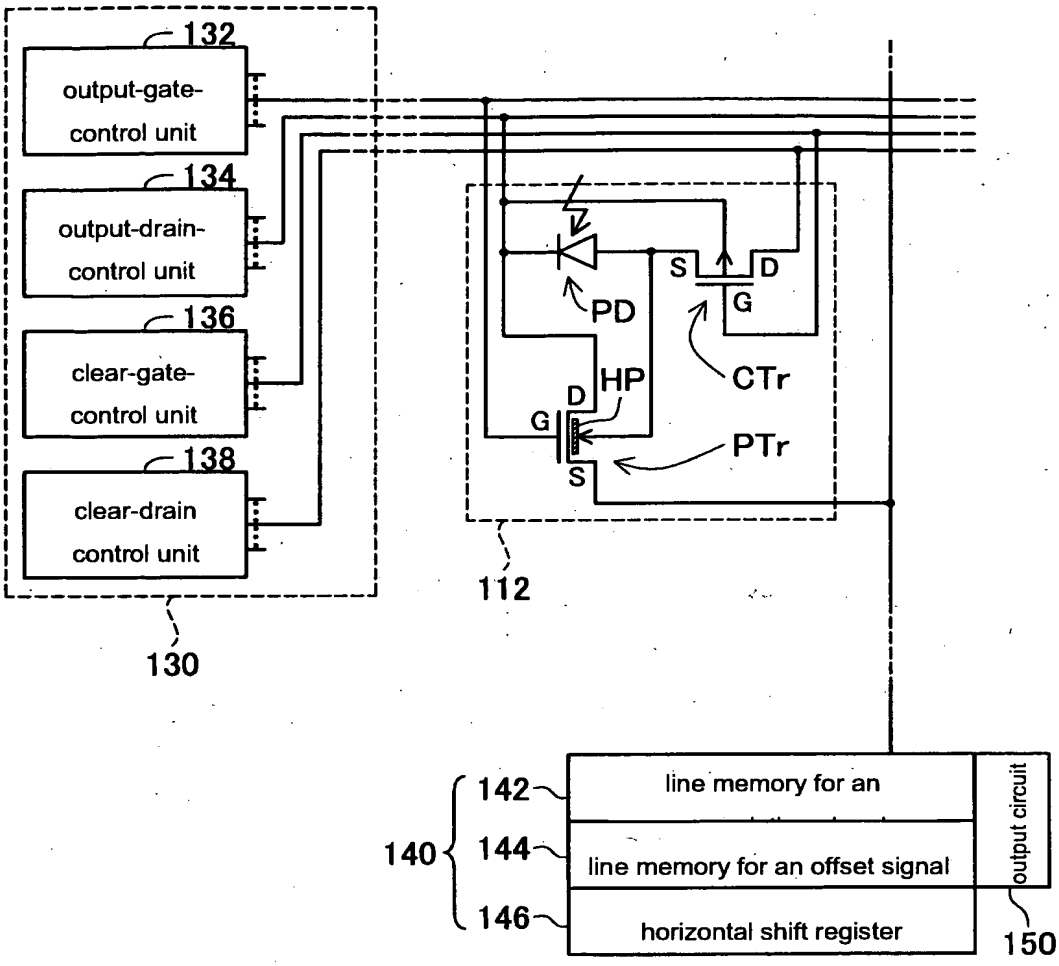
132
output-gate-control unit
134
output-drain-control unit
136
clear-gate-control unit
138
clear-drain control unit
130
112
PD
S
D
G
CTr
HP
D
G
S
PTr
140
142
line memory for an
144
line memory for an offset signal
146
horizontal shift register
output circuit
150

FIG.3

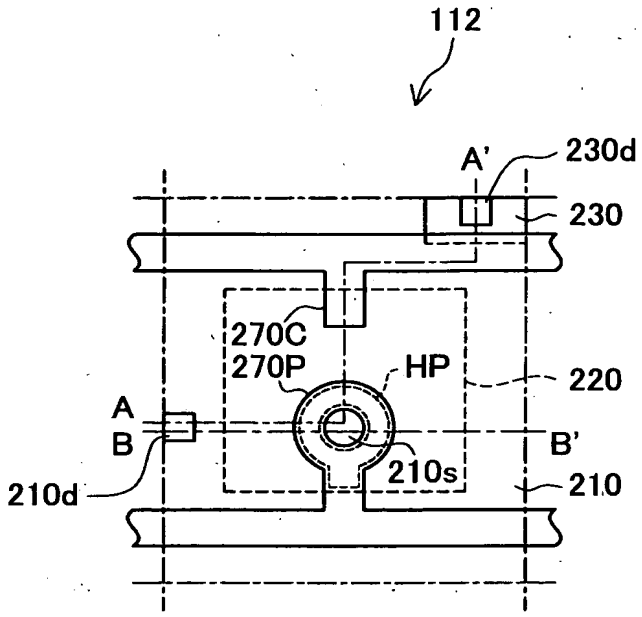
112
A'
230d
230
270C
270P
HP
220
A
B
B'
210s
210d
210

FIG.4

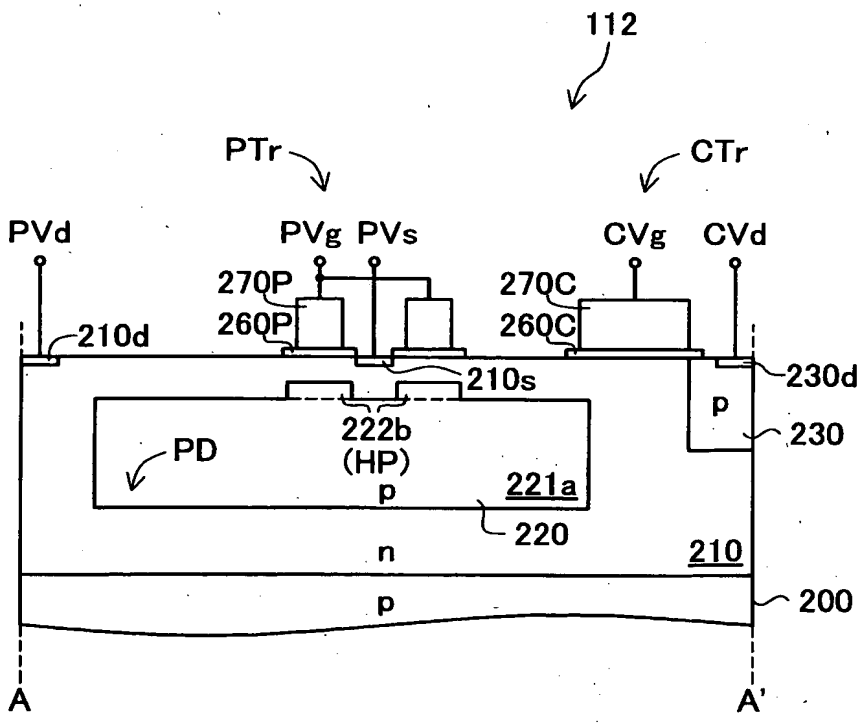
112
PTr
CTr
PVd
PVg
PVs
CVg
CVd
270P
260P
270C
260C
210d
210s
230d
p
230
222b
(HP)
PD
p
221a
220
n
210
p
200
A
A'

FIG.5

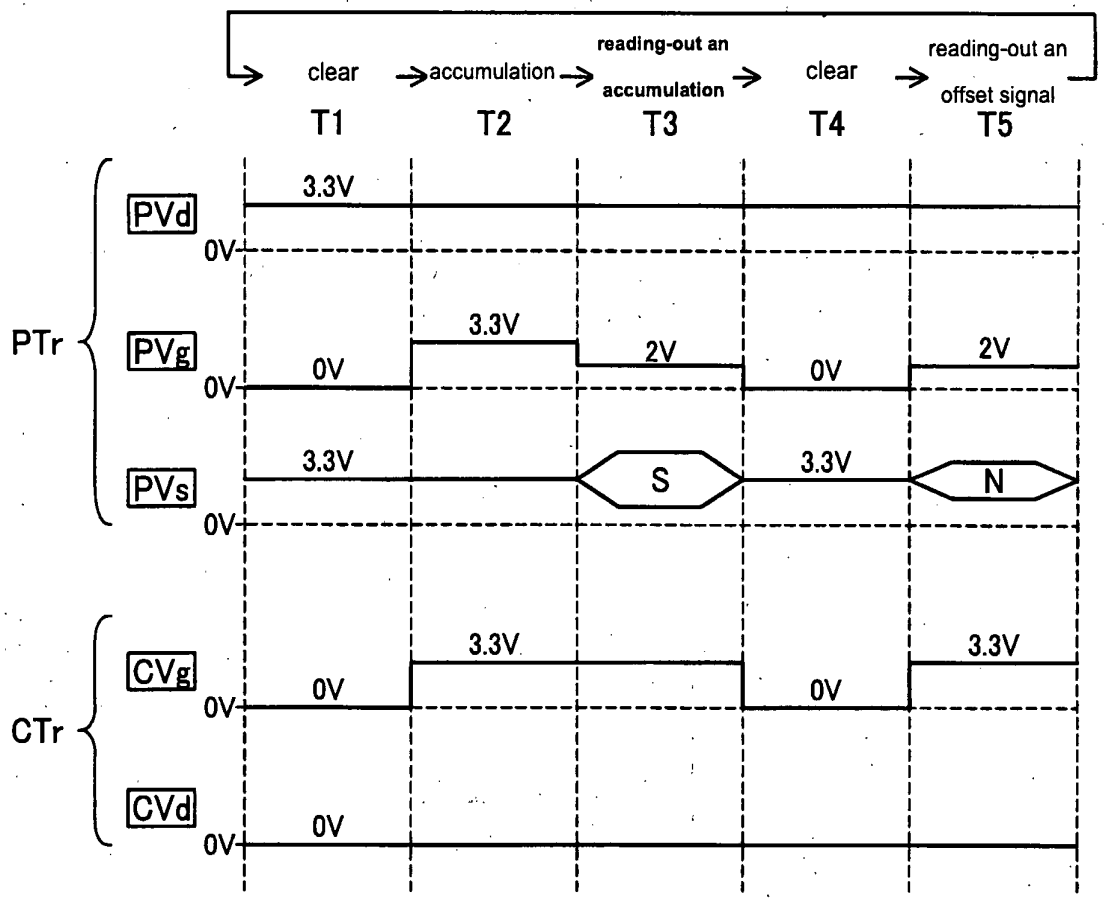
clear
accumulation
reading-out an accumulation
clear
reading-out an offset signal
T1
T2
T3
T4
T5
PTr
PVd
PVg
PVs
CTr
CVg
CVd
3.3V
0V
2V
S
N

FIG.6

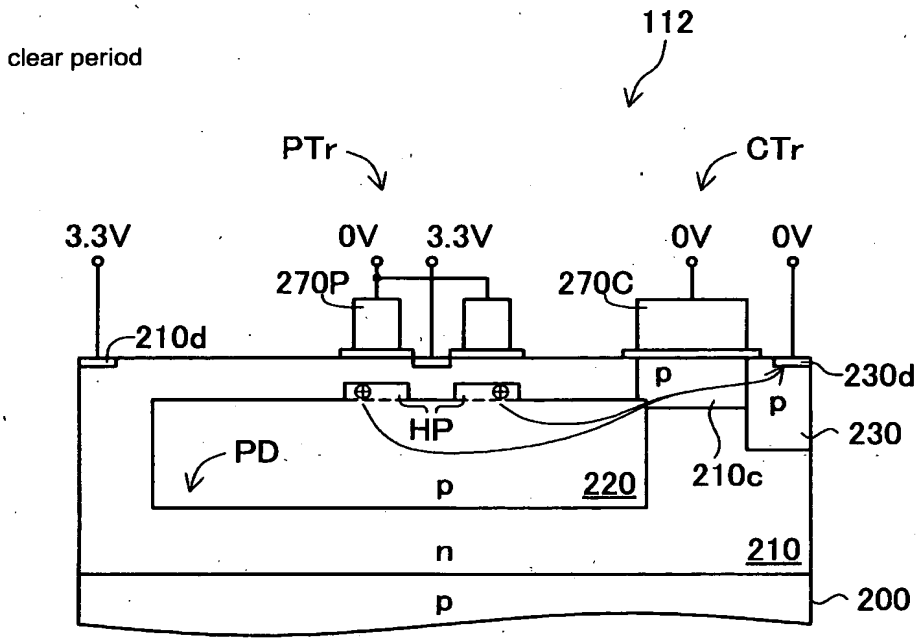
clear period
112
PTr
CTr
3.3V
0V
3.3V
0V
0V
270P
270C
210d
230d
p
p
HP
230
PD
p
220
210c
n
210
p
200

FIG.7

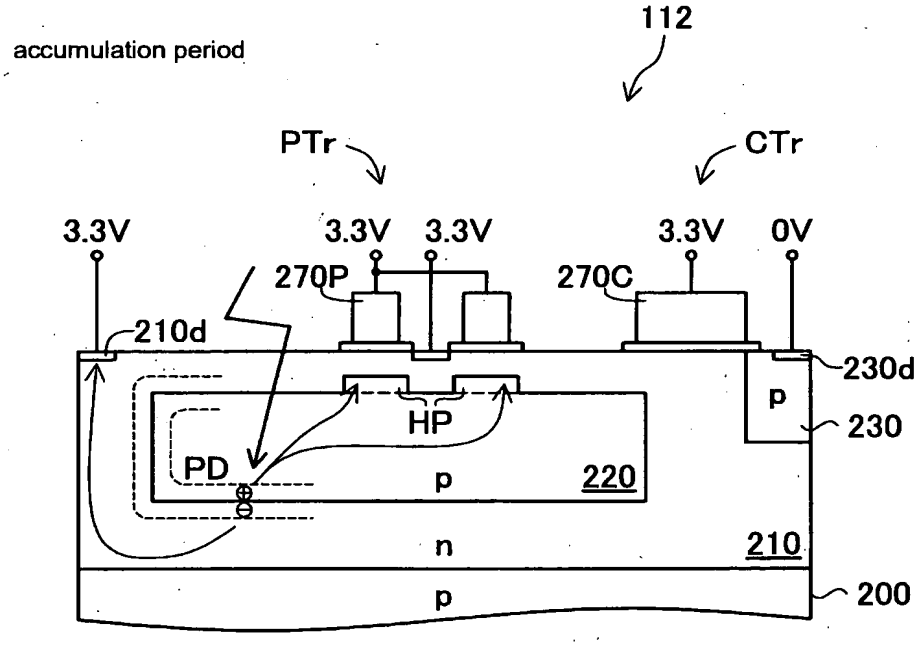
accumulation period
112
PTr
CTr
3.3V
3.3V
3.3V
3.3V
0V
270P
270C
210d
230d
p
HP
230
PD
p
220
n
210
p
200

FIG.8

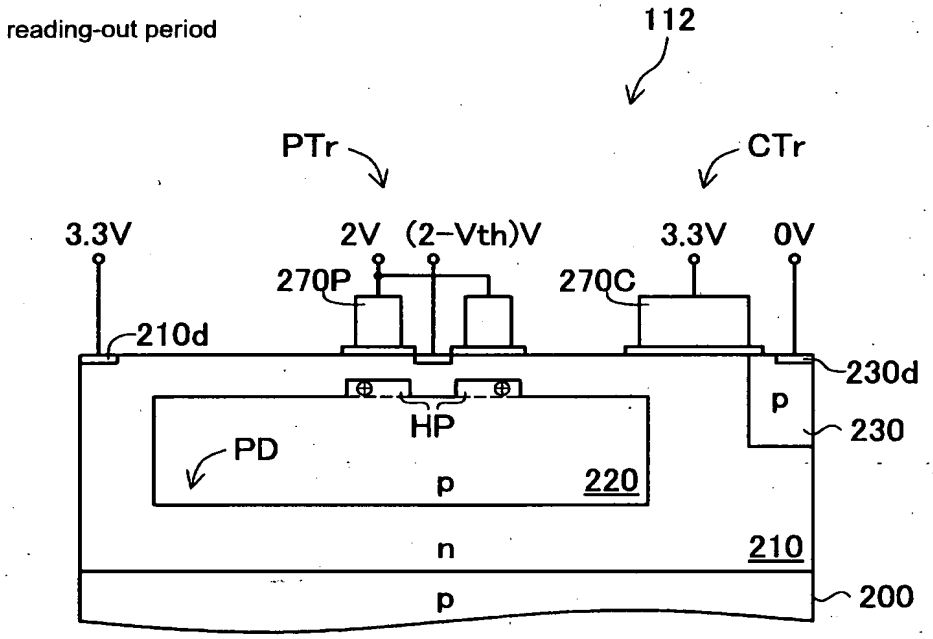
reading-out period
112
PTr
CTr
3.3V
2V
(2-Vth)V
3.3V
0V
270P
270C
210d
230d
p
230
HP
PD
p
220
n
210
p
200

FIG.9A

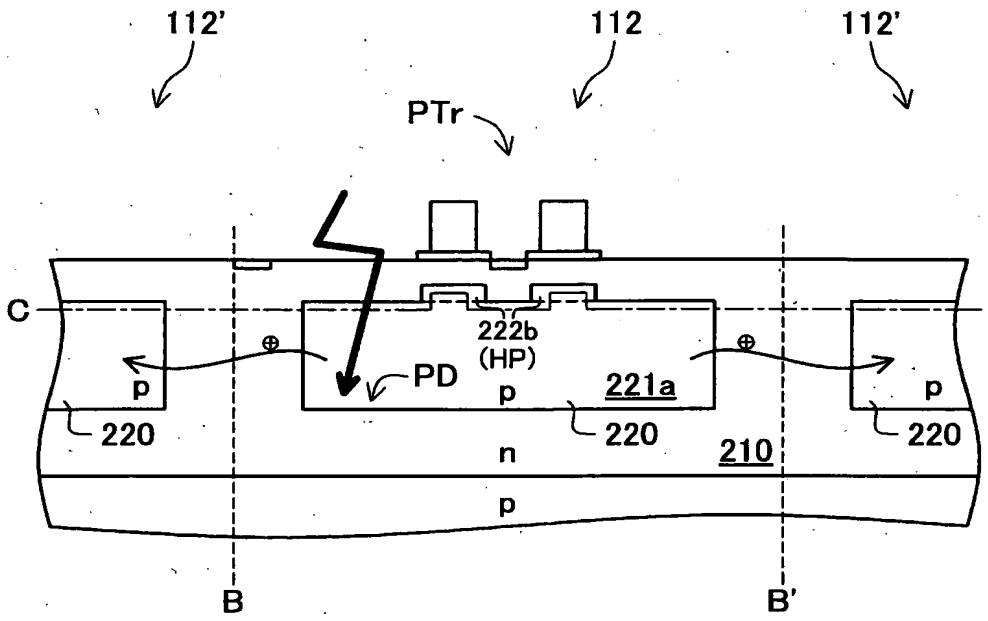
112'
112
112'
PTr
C
222b
(HP)
PD
p
221a
p
p
220
220
220
n
210
p
B
B'

FIG.9B

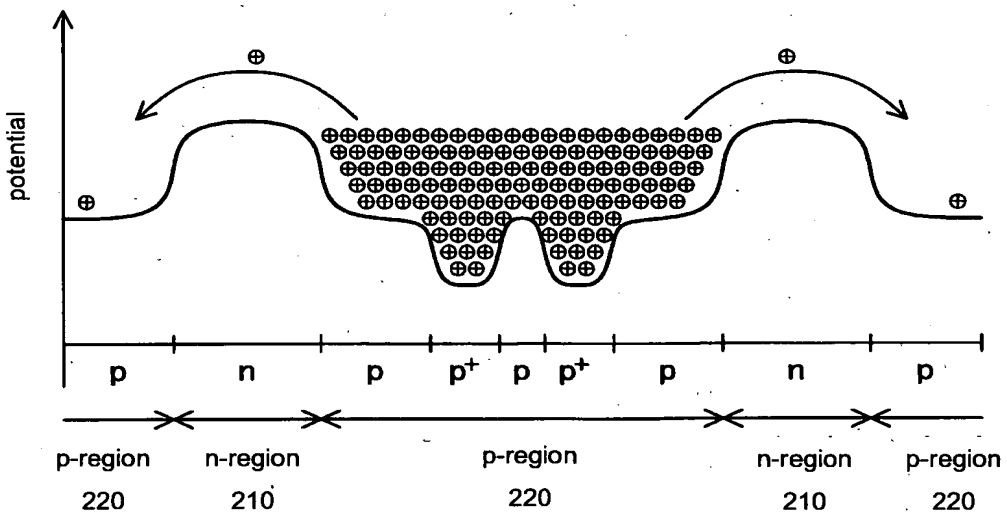
potential
p
n
p
p+
p
p+
p
n
p
p-region
220
n-region
210
p-region
220
n-region
210
p-region
220

FIG.10

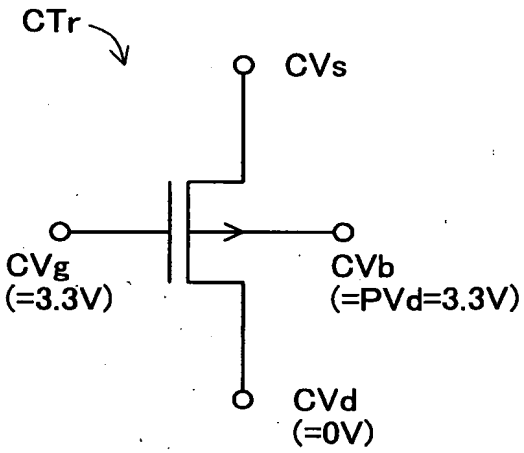
CTr
CVs
CVg
(=3.3V)
CVb
(=PVd=3.3V)
CVd
(=0V)

FIG.11

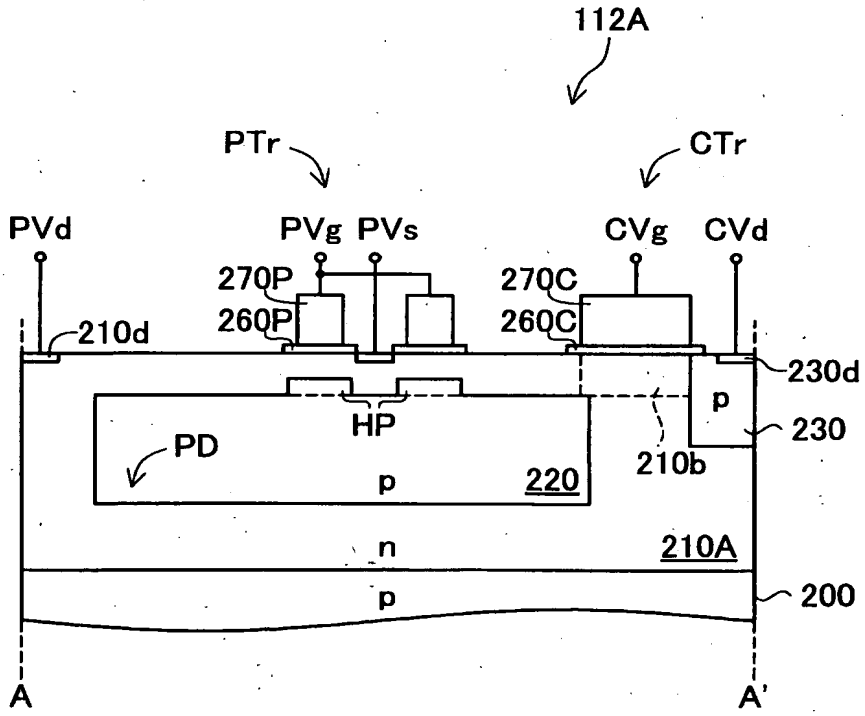
112A
PTr
CTr
PVd
PVg
PVs
CVg
CVd
270P
260P
270C
260C
210d
230d
p
230
HP
210b
PD
p
220
n
210A
p
200
A
A'

FIG.12A

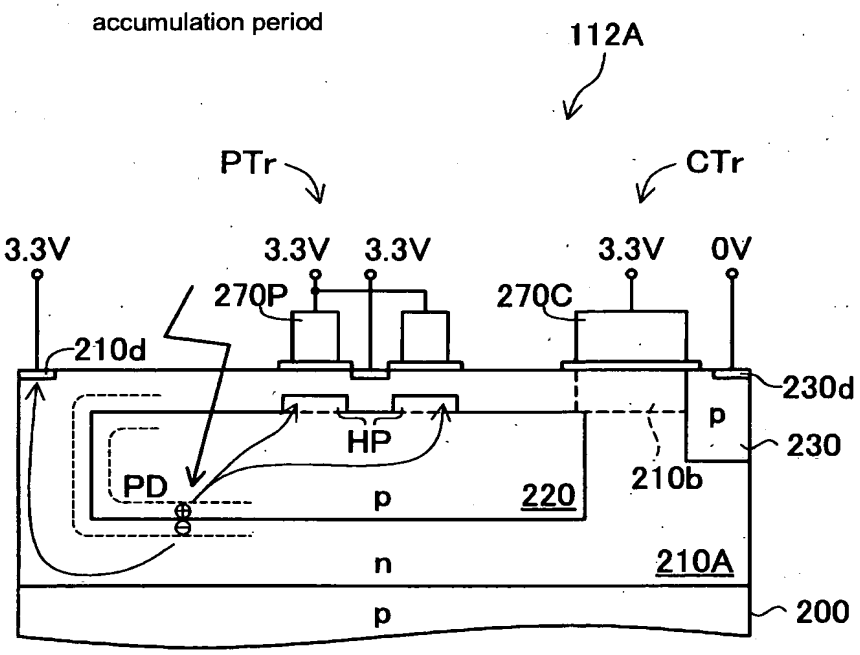

FIG.12B

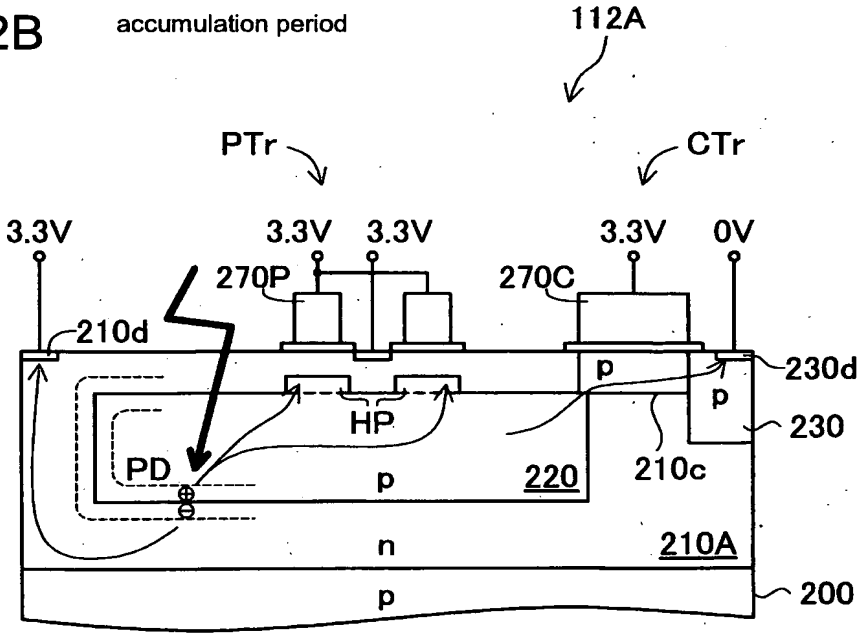

FIG.13

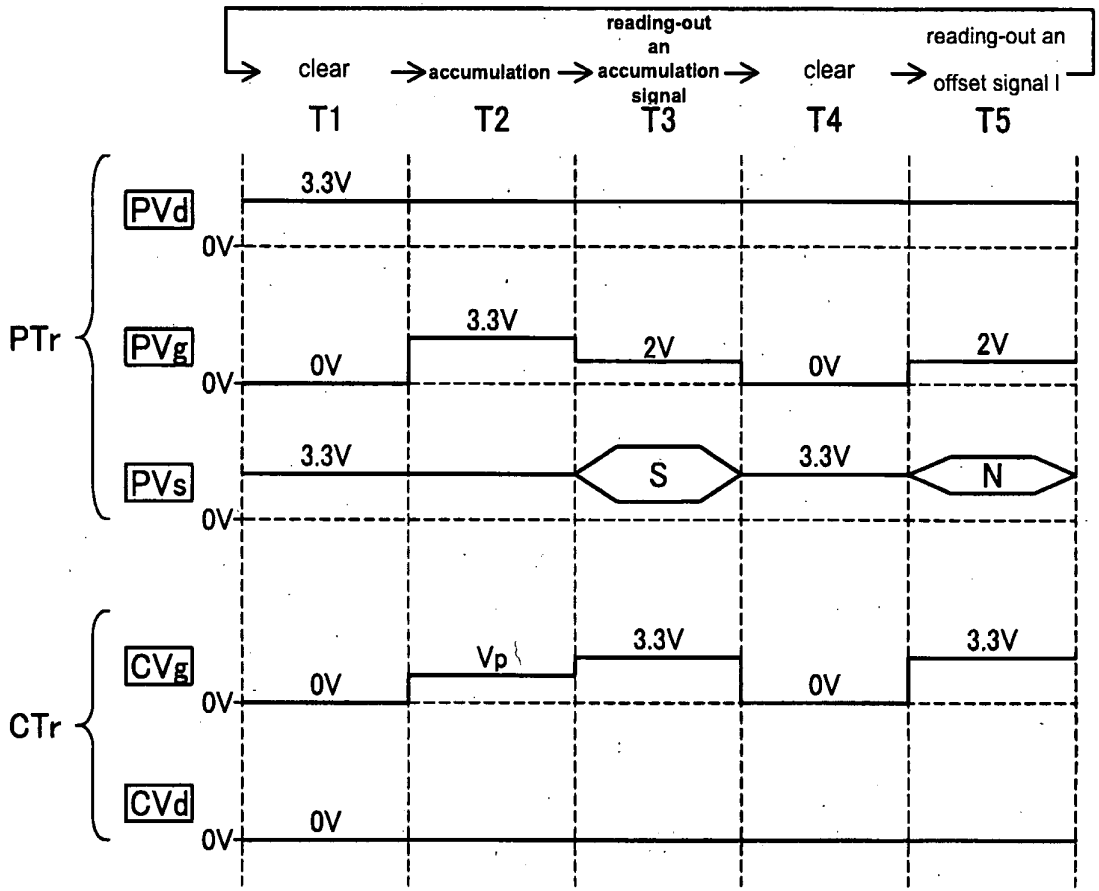
clear
accumulation
reading-out an accumulation signal
clear
reading-out an offset signal I
T1
T2
T3
T4
T5
PTr
PVd
PVg
PVs
CTr
CVg
CVd
3.3V
0V
2V
S
N
Vp

FIG.14A

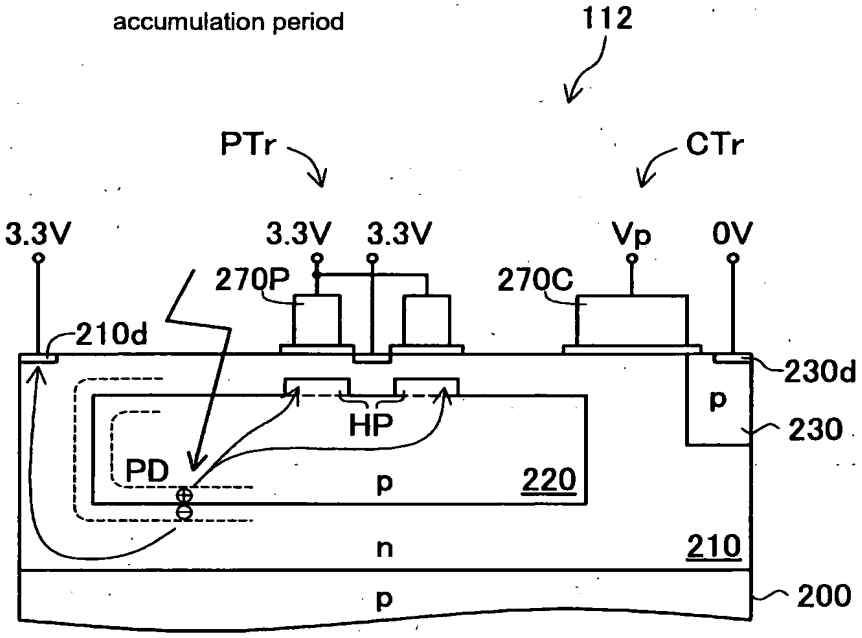

FIG.14B